REMARKS

Claims 1 and 3-12 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejection(s) in view of the amendments and remarks contained herein.

SPECIFICATION

The title of the invention stands objected to as not being descriptive. Applicants have amended the title to be more descriptive as requested. Applicants respectfully assert that the amendment to the title provided herein obviates this rejection.

CLAIM OBJECTIONS AND REJECTION UNDER 35 U.S.C. § 112

Claims 4-12 stand objected to under 37 CFR 1.75(c) as being in improper form due to multiple dependent claim 3. In addition, Claims 4-12 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for filing to particularly point and distinctly claim the subject matter which Applicant regards as the invention.

Applicants have amended the claims herein to eliminate the multiple dependency. Consequently, the claims are now in proper form obviating this objection and this rejection.

REJECTIONS UNDER 35 U7.S.C. § 102

Amended claim 1 of the present invention recites "the active region is configured by alternately layering: first semiconductor layers provided in plurality which functions as a carrier transit region, and second semiconductor layers, which is composed of δ doped layers provided in plurality, which includes a higher concentration of impurities for carriers than the first semiconductor layer, and which has a thinner film thickness than the first semiconductor layer; wherein the first semiconductor layers and the second semiconductor layers are made of the same material; wherein each of the first semiconductor layers has the same thickness; and wherein the concentration of impurities for carriers included in the second semiconductor layers is substantially constant". Hence as shown in page 21, line 16 to page 22, line 20 of the present specification, carriers are migrated from the second semiconductor layers composed of δ doped layers to either undoped first semiconductor layers or first semiconductor layers having a carrier concentration lower than that of the second semiconductor layers. As a result, carriers can travel through the undoped first semiconductor layers or the first semiconductor layers having a carrier concentration lower than that of the second semiconductor layers, and the resistance value of the plurality of δ doped layers can be reduced. Moreover, since the plurality of δ doped layers are depleted during the OFF state, a high withstand voltage value can be obtained.

1. Hiroyuki

Claims 1-2, 4-5, and 11-12 stand rejected under 35 U.S.C. 102(b) as being anticipated by Hiroyuki et al (JP. 06-349860). Applicants respectfully traverse this rejection.

Cited reference JP6-349860 (hereafter Hiroyuki) teaches, during the alternate deposition of undoped GaAs layers 4 and δ doped layers 5, a channel layer is deposited by either increasing the concentration of carriers in the δ doped layers 5 towards a semiconductor surface opposite to a semi-insulative substrate 1 or decreasing the interval of the δ doped layers 5 towards the semiconductor surface opposite to the semi-insulative substrate 1, such that the center of mass of the concentration of the carriers exists in the gate electrode 8 side.

However according to the present invention, the concentration of impurities for carriers included in the second semiconductor layers, which is composed of δ doped layers, is substantially constant. Moreover, since each of the first semiconductor layers of the present invention has the same thickness, the intervals of the second semiconductor layers composed of δ doped layers are substantially constant. Hence, the present invention is different from Hiroyuki.

Further, Hiroyuki merely discloses that the center of mass of the concentration of the carriers exists in the gate electrode 8 side; but fails to teach or suggest that the carriers are migrated from the second semiconductor layers composed of δ doped layers to the first semiconductor layers.

For the foregoing reasons, the present invention is patentable over Hiroyuki.

2. Suzuki

Claims 1-2, 4-5, and 12 stand rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki (JP. 5-13446). This rejection is respectfully traversed.

The cited reference JP5-13446 (hereafter Suzuki) teaches alternately depositing undoped GaAs layers 141-146 and δ doped layers 151-155 composed of Si-doping layers. Suzuki also discloses that each of the δ doped layers 151-155 has the same thickness. According to paragraphs [0013] - [0014] of Suzuki, an i-GaAs layer 141 not doped by impurities and which has a thickness of 6nm is deposited on a barrier layer 13. Thereafter, the shutter of a Ga vaporizer, which is opened due to the process of depositing the i-GaAs layer 141, is closed, and at the same time or after a few seconds, the shutter of a Si vaporizer is opened for 60 seconds to deposit a Si doping layer 151, such that one δ doped layer is deposited. Next, the shutter of the Si vaporizer is closed and the shutter of the Ga vaporizer is opened to deposit a 6nm i-GaAs layer 142. This process is repeated until all the i-GaAs layers 141-145 (14) not doped by impurities and the Si doping layers 151-155 (15) are alternately deposited to form a multilayer structure.

Since after depositing the 6nm i-GaAs layer 141, the shutter of the Ga vaporizer is closed and the shutter of the Si vaporizer is opened to deposit the Si doping layer 151, the Si doping layer 151 is composed of Si and As and does not include Ga.

However according to the present invention, the first semiconductor layers and the second semiconductor layers are made of the same material (for example, SiC). Hence, the present invention is patentable over Suzuki.

Further, paragraph [0025] of Suzuki discloses that the concentration of the sheet carrier increases due to the difficulty of electrons moving into the AlGaAs layers 13 and 16 having wide forbidden band, and electrons are trapped in the GaAs layer 14. However, considering the difficulty of electrons moving into the AlGaAs layers 13 and 16 having wide forbidden band and the Figs., the GaAs layer 14, in which electrons are trapped, refers to the GaAs layer and the entire Si doping layer 15 sandwiched between the AlGaAs layers 13 and 16. Hence, Suzuki discloses that the concentration of the sheet carriers increases due to the difficulty for electrons to move into the AlGaAs layers 13 and 16 having wide forbidden band, and electrons are trapped in the GaAs layer 14 and the entire Si doping layer 15.

However, Suzuki fails to teach or suggest the respective changes of the GaAs layer 14 and the Si doping layer 15. Hence, Suzuki completely fails to teach or suggest about the migration of the carriers from the Si doping layer 15.

Moreover, conventionally, in order for the carriers to migrate from the δ doped layers, the first semiconductor layers and the second semiconductor layers composed of δ doped layers must be made of the same material.

If the materials of the first and second semiconductor layers are different, the band gap of each layer would be different. Hence, due to the first and second semiconductor layers, a potential well (quantum well), in which the carriers are trapped, is formed, and the migration of the carriers can hardly occur.

Hence, the present invention is patentable over Suzuki.

3. Semichon

Claims 1-5 stand rejected under 35 U.S.C. 102(b) as being anticipated by Semichon et al (US. 3,739,243). This rejection is respectfully traversed.

The cited reference USP 3,739,243 (hereafter Semichon) teaches a semiconductor composed of a first semiconductor layer 3 composed of GaAs, which includes low concentration of carriers, and a second semiconductor layer 2 composed of GaAs, which includes high concentration of carriers, and the first semiconductor layer is in contact with the second semiconductor layer.

However, the first and second semiconductor layers each both consist of only one layer. Moreover, Semichon fails to disclose that the second semiconductor layer, which has high concentration of carriers, is composed of a δ doped layer. This is because according to Semichon, the thickness of the second semiconductor layer is 1 micron (column 3, line 25) and 0.2 micron (= 200nm) (column 3, line 54). Hence there is no motivation in forming a δ doped layer by selectively doping impurities into the extremely thin region of the layer. Further, even considering that the substrate 4 is heavily doped, it is obvious that the thickness of the first semiconductor layer 3 is different from that of the second semiconductor layer 2.

For the foregoing reasons, the present invention is patentable over Semichon.

4. Sumino

Claims 1-2 and 5 stand rejected under 35 U.S.C. 102(b) as being anticipated by Sumino et al (JP. 54-132173). This rejection is respectfully traversed.

Cited reference JP54-132173 (hereafter Sumino) teaches a semiconductor composed by laminating a n layer 22 including low concentration of carriers, a n+

layer 23 including high concentration of carriers, and a n layer 24 including low concentration of carriers.

However, the n+ layer 23 that corresponds to the second semiconductor layers of the present invention is composed of only one layer. Moreover, according to Fig. 2 of Sumino, each of the n layers 22 and 24, which correspond to the first semiconductor layers of the present invention, has a different thickness.

In addition, Sumino fails to disclose that the n+ layer 23, which corresponds to the second semiconductor layers of the present invention, is composed of a δ doped layer, and fails to disclose other detail descriptions of the n+ layer 23. Hence, there is no motivation in forming a δ doped layer by selectively doping impurities into the extremely thin region of the layer.

Therefore, the present invention is patentable over Sumino.

REJECTION UNDER 35 U.S.C. § 103

1. Sumino in view of Odekirk

Claims 3-4 and 6-8 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Sumino et al in view of Odekirk (US. 6,388,272). This rejection is respectfully traversed.

Odekirk fails to disclose or suggest the missing features discussed above with respect to Sumino. Thus, this combination of references fails to teach the features of applicants invention discussed above. Further, like Suzuki, all of the cited references fail to disclose that the first semiconductor layers and the second semiconductor layers composed of δ doped layers are made of the same material,

and that the carriers migrate from the second semiconductor layers composed of δ doped layers. Therefore, Applicants' invention is also patentable over this combination of references.

2. Semichon in view of Odekirk

Claims 6-7 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Sumino et al in view of Odekirk (US. 6,388,272).

Odekirk fails to disclose or suggest the missing features discussed above with respect to Semichon. Thus, this combination of references fails to teach the features of applicants invention discussed above. Also as indicated in Applicants response previous rejection, all of the cited references fail to disclose that the first semiconductor layers and the second semiconductor layers composed of δ doped layers are made of the same material, and that the carriers migrate from the second semiconductor layers composed of δ doped layers. Therefore, applicants invention is also patentable over this combination of references.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is

respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: 3 DEC 02

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ATTACHMENT FOR CLAIM AMENDMENTS

The following is a marked up version of each amended claim in which underlines indicates insertions and brackets indicate deletions.

1. (Amended) A semiconductor device made by providing on a substrate an active region that functions as a portion of an active element,

wherein the active region is configured by alternately layering:

[at least one] first semiconductor [layer] layers provided in plurality which [is provided on the substrate, and which] functions as a carrier transit region, and

[at least one] second semiconductor [layer] layers, which is composed of δ doped layers provided in plurality, which includes a higher concentration of impurities for carriers than the first semiconductor layer, and which has a thinner film thickness than the first semiconductor layer[, and from which carriers can migrate to the first semiconductor layer due to quantum effects];

wherein the first semiconductor layers and the second semiconductor layers are made of the same material;

wherein each of the first semiconductor layers has the same thickness; and

wherein the concentration of impurities for carriers included in the second semiconductor layers is substantially constant.

3. (Amended) The semiconductor device according to claim 1 [or 2],

wherein the concentration of impurities for carriers in the first semiconductor layer is below 1×10^{17} atoms $\cdot$ cm^{-3}, and

wherein the concentration of impurities for carriers in the second semiconductor layer is at least 10^{17} atoms $\cdot$ cm^{-3}.

4. (Amended) The semiconductor device according to [any of claims] claim 1 [to 3], wherein the substrate an the active region are made of one material selected from SiC, GaN, and GaAs.

5. (Amended) The semiconductor device according to [any of claims] claim 1 [to 3], wherein the first and second semiconductor layers in the active region are made of the same material.

6. (Amended) The semiconductor device according to [any of claims] claim 1 [to 3],

wherein the second semiconductor layer is a SiC layer, and

wherein the thickness of the second semiconductor layer is at least one monolayer and below 20 nm.

7. (Amended) The semiconductor device according to [any of claims] claim 1 [to 3],

wherein the first semiconductor layer is a SiC layer, and

wherein the thickness of the first semiconductor layer is at least about 10 nm and at most about 100 nm.

8. (Amended) The semiconductor device according to [any of claims] claim 1 [to 7],

wherein the substrate is a semiconductor layer that includes a high concentration of impurities,

wherein the uppermost portion of the active region is made of the first semiconductor layer, and

wherein the semiconductor device further comprises a Schottky electrode providing a Schottky contact with a portion of the upper surface of the first semiconductor layer at the uppermost portion of the active region, and

an ohmic electrode providing an ohmic contact with a portion of the substrate.

9. (Amended) The semiconductor device according to [any of claims] claim 1 [to 7], further comprising:

a Schottky electrode providing a Schottky contact with a first lateral face of the first semiconductor layer and of the second semiconductor layer of the active region, and

an electrode that is connected to a second lateral face of the first semiconductor layer and of the second semiconductor layer of the active region, the second lateral face being arranged at a certain spacing from the first lateral face.

11. (Amended) The semiconductor device according to [any of claims] claim 1 [to 7], wherein the uppermost portion of the active region is made of the first semiconductor layer, and

wherein the semiconductor device further comprises:

a Schottky gate electrode, which is in Schottky contact with a portion of the upper surface of the first semiconductor layer at the uppermost portion of the active region, and

source and drain electrodes, which are provided on the active region and sandwich the Schottky gate electrode, and which are connected to the active region.